

**OCT 12 2006**

Appl. No. 10/733,984  
Examiner: MONDT, JOHANNES P, Art Unit 3663  
In response to the Office Action dated July 18, 2006

Date: October 12, 2006  
~~Attorney Docket No. 10113311~~

**AMENDMENTS TO THE CLAIMS**

This listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims**

Claim 1-22 (cancelled)

Claim 23 (currently amended): A structure for a bit line contact hole, comprising:

a substrate ;

a transistor, disposed on the substrate, comprising a gate layer covered by a first insulating layer and comprising a doped region;

an inner landing pad, disposed on the doped region and parts of the transistor, comprising a polysilicon layer;

a passivation layer serving as a diffusion barrier, ~~disposed on~~ conformally formed on the inner landing pad, the transistor, and the substrate;

a second insulating layer comprising doped materials, disposed on the passivation layer, having a flat surface on the passivation layer;

a contact plug, disposed on the second insulating layer and the passivation layer and contacted with the inner landing pad, electrically connecting with the inner landing pad; and

an interconnected landing pad, deposited on the contact plug.

Claim 24 (previously presented): The structure as claimed in claim 23, wherein thickness of the polysilicon layer of the inner landing pad is about 100~400Å.

Claim 25 (previously presented): The structure as claimed in claim 23, wherein the material of the passivation layer comprises silicon nitride.

Claim 26 (previously presented): The structure as claimed in claim 25, wherein thickness of the passivation layer is about 110~130Å .

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Claim 27 (withdrawn): A structure for a bit line contact hole, comprising:

a substrate ;

a transistor, disposed on the substrate, comprising a gate layer covered by a first insulating layer and comprising a doped region;

an inner landing pad, disposed on the doped region and parts of the transistor, comprising a polysilicon layer;

a passivation layer, disposed on the inner landing pad, the transistor, and the substrate, the passivation layer has a thickness of about 110~130Å;

a second insulating layer, disposed on the passivation layer, having a flat surface on the passivation layer;

a contact plug, disposed on the second insulating layer and the passivation, electrically connecting with the inner landing pad; and

an interconnected landing pad, deposited on the contact plug.